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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,516	08/22/2003	Koji Ono	0756-7186	8778

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/645,516	ONO ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/714,891.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The disclosure is objected to because of the following informalities:

Page 1, line 2: please insert the information of the parent application.

Page 16, line 15: the reference sign of the resist "1009" should be changed to --1007--.

Page 17, line 6: the reference sign of the enlarged view of the region "1017" should be changed to --1013--.

Page 19, lines 8-10: please insert the following reference signs:

Line 8, after first impurity region, insert the reference sign –1026--

Line 9, after LDD region, insert the reference sign --1025—

Line 10, after LDD region, insert the reference sign --1024--

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-4, 6, 10, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima et al. (US Pat. No. 6,001,714) in view of Sera (US Pat. No. 6,287,898 B1).

Regarding claims 1-4, Nakajima et al. teaches a conventional embodiment of forming a TFT comprising the steps of:

a first step of forming an insulating film (16) on a semiconductor layer (12a) (see, fig. 15a);

a second step of forming a conductive layer (18a) on the insulating film (see fig.15a));

a third step of selectively etching the conductive layer (18a) (see figs. 1a and 1b, col. 6, lines 28-33 and col. 9, lines 66-67), forming conductive layer having a first tapered shape (consider the tapered shaped of the gate 18a in figure 15a);

a fourth step of doping a single conductivity type impurity element (dopant) into the semiconductor layer (13 and 14), after completing the third step (see Fig. 15b and col. 10, lines 1-3);

a fifth step of selectively etching the conductive layer (18a) having the first tapered shape, forming a conductive layer having a second tapered shape (18) (see fig. 15c and col. 10, lines 3-6. Please note that the width of gate 18 is smaller than the width of the gate 18a); and

a sixth step of forming a low concentration region (83) in the semiconductor layer (see fig. 15d).

In addition and with regards to claim 4, Nakajima et al. teaches that it is well known in the art to provide a TFT in each pixel of the pixel portion (consider the TFT as a switch for a pixel element in col. 1, lines 24-37).

However, the conventional embodiment of Nakajima et al. fails to teaches the step doping a single conductivity type impurity element into the semiconductor layer, after completing the fifth step, wherein the concentration of the single conductivity type impurity element doped in the sixth step is lower than the concentration of the single conductivity type impurity element doped in the fourth step. In addition and with respect to claim 2, the conventional embodiment of Nakajima et al. is silent with respect to the conductivity of the TFT transistor. Finally and with regards to claim 3, the conventional embodiment of Nakajima et al. is silent with respect to performing a first step of forming an insulating film on the N-channel TFT and P-channel TFT, and a seventh step of doping an impurity element, having a conductivity type which is inverse to the

conductivity type of the single conductivity type element, into the semiconductor layer of the p-channel thin film transistor, after completing the sixth step.

Sera teaches lightly doping a low concentration region (11) in the semiconductor layer (3) (see fig. 3D and col. 5, lines 25-29), after forming a highly doped concentration region (7) (see fig. 3B) and after forming a second mask (13) having a reduced width (see fig. 3C). Please note that region (11) is a LDD region, which has a concentration that is lower than the concentration of a source/drain region (7) (col. 4, lines 61-65 and col. 5, lines 25-29).

In addition and with regards to claim 2, Sera teaches that it is well known in the art to implant N-type impurities in the semiconductor layer (3) to form a n-channel TFT having a n-type source/drain region (7) and a n-type LDD region (11) (see col. 4, lines 61-65 and col. 5, lines 23-28).

Further and with regards to claim 3, Sera teaches that it is well known in the art to form a CMOS TFT structure (col. 6, lines 51-52) by forming an insulating film (4) on a semiconductor layer (3) of the N-channel TFT (17) and on a semiconductor layer (3) of the P-channel TFT (18) (see fig. 5A) and by doping an impurity element having a conductivity type (consider the P-type impurity element 29 shown in figure 5F that defines the LDD region 11 of the p-channel transistor 18), which is inverse to the conductivity type of the single conductivity type element (consider the N-type impurity element 28 shown in figure 5E that defines the LDD region 11 of the n-channel transistor 17), into the semiconductor layer (3) of the p-channel thin film transistor (18)

(see fig. 5F), after implanting the N-type LDD region (11) (see fig. 5E), which was implanted after the implantation of the N-type source/drain region (7) (see fig. 5B).

Nakajima et al. and Sera are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an N-channel TFT or a CMOS TFT by including a first step of forming an insulating film on a semiconductor layer of the N-channel TFT and P-channel TFT; a sixth step of doping a single conductivity type impurity element into the semiconductor layer, after completing the fifth step; and a seventh step of doping an impurity element, having a conductivity type which is inverse to the conductivity type of the single conductivity type element, into the semiconductor layer of the p-channel thin film transistor, after completing the sixth step; wherein the concentration of the single conductivity type impurity element doped in the sixth step is lower than the concentration of the single conductivity type impurity element doped in the fourth step. The motivation for doing so is forming an LDD region to reduce leakage current and manufacturing cost by reducing the number of steps (col. 9, lines 51-53 of Sera). Therefore, it would have been obvious to combine Sera with Nakajima et al. to obtain the invention of claims 1-4, 6, 10, 11 and 12.

Regarding claims 6, 10, 11 and 12, Nakajima et al. teaches forming the gate electrode (8a) of W-alloy (see col. 6, lines 24-25).

6. Claims 5, 7-9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima et al. (US Pat. No. 6,001,714) in view of Sera (US Pat. No. 6,287,898 B1), and further in view of Ishida (US Pat. No. 6,534,789 B2).

Regarding claims 5 and 7-9, a further difference between the prior art and the claimed invention is the limitation that the tapered portion of the gate electrode has a angle greater than or equal to 30° and less than or equal to 60°.

Ishida further teaches that it is well known in the art to form the tapered portion of the gate electrode (15) having an angle of greater than or equal to 30° and less than or equal to 60° (consider the angle of 35° in col. 13, lines 39-40 and the range 20°-70° in col. 10, lines 60-63).

Nakajima et al., Sera and Ishida are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the tapered portion of the gate electrode having an angle of greater than or equal to 30° and less than or equal to 60°. The motivation for doing so, as is taught by Ishida, is to improve the step coverage of the insulating film (col. 10, lines 54-56). Therefore, it would have been obvious to combine Ishida with Nakajima et al. and Sera to obtain the invention of claims 5, 7-9 and 13.

Regarding claim 13, Nakajima et al. teaches forming the gate electrode (8a) of W-alloy (see col. 6, lines 24-25).

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

2/19/05

José R. Díaz
Examiner
Art Unit 2815